A 33mW 8Gb/s CMOS Clock Multiplier and CDR for Highly Integrated I/Os

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Abstract

A 0.622-8 Gb/s CDR circuit using injection locking for jitter suppression and phase interpolation in high bandwidth SOC solutions is described. A Slave Injection Locked Oscillator (SILO) is locked to a Tracking Aperture-Multiplying DLL (TA-MDLL) via a coarse phase selection MUX. For the fine timing vernier, an interpolator DAC controls the injection strength of the MUX output into the SILO. This 1.2V 0.13µm CMOS CDR consumes 33mW@8Gb/s. Die area including voltage regulator is 0.08mm^2. Recovered clock jitter is 6.9ps rms/49.3ps peak-to-peak at a 200ppm bitrate offset.

Introduction

In order to integrate large numbers of transceivers on a single chip, the constraints of power, area and supply noise become more acute. Other concerns include substrate noise induced jitter and adjacent oscillator coupling. A Multiplying DLL (MDLL) architecture has been used here in order to alleviate some of these concerns, where a reference clock, when multiplexed in, can reset any accumulated jitter to zero [1]. However, the MDLL timing circuitry gating the incoming reference clock edge has to be precise [1] and can limit the maximum MDLL oscillation frequency. The timing aperture in which the buffered reference clock edge (RCLK) is multiplexed in must be maximized to account for jitter, and centered around the clean clock edge across process, voltage, temperature, (PVT) and operating frequency. A design incorporating a Tracking Aperture-MDLL (TA-MDLL) is used to ensure robustness in multiplexing in a clean clock edge. When the accumulated jitter is reset, duty-cycle distortion invariably occurs at the output of the TA-MDLL. This deterministic form of jitter can be filtered out by injection locking [2] a slave oscillator (SILO) to the TA-MDLL. The relative strength of the injection into each SILO delay element can be varied to perform phase interpolation for clock recovery.

Architecture

Fig. 1 shows the architecture of the CDR where it incorporates the TA-MDLL as a clock multiplier. The clock multiplier can multiply a reference clock up to M = 1X, 2X, 4X, 5X, 8X, 10X the original frequency. With 4:1 serial I/O mux/demux [3], 8Gb/s operation can be achieved with a clock frequency of 2GHz. Upon startup, the Pulser and Phase Detector/Charge Pump (PD/CP) is turned off while the MDLL acts like a ring oscillator until the Frequency Acquisition block can acquire the correct frequency. In this mode, the loop acts as a PLL where it avoids the duty-cycle distortion of the MDLL but has greater jitter due to accumulation. When the Frequency Acquisition circuitry detects a frequency within 1% of the desired value, it signals the Pulser and PD/CP to begin operation. Fig. 2(a) shows that the pulser is made up of delay elements that are delay matched to the delay elements in the MDLL and the SILO. This is important as it allows for the maximum available SEL aperture to multiplex in RCLK and ensures that RCLK is centered within the SEL aperture as shown in Fig. 2(b). For 2GHz MDLL oscillation, the clock period is 500ps or 4 Unit Intervals (UI), and since there are 8 MDLL phases, the propagation delay of each delay element in the MDLL and Pulser is 62.5ps (0.5UI) if they are all matched. Thus when a clean RFC edge enters the pulser, it is shaped into the RCLK pulse that is tracked by the SEL aperture. This

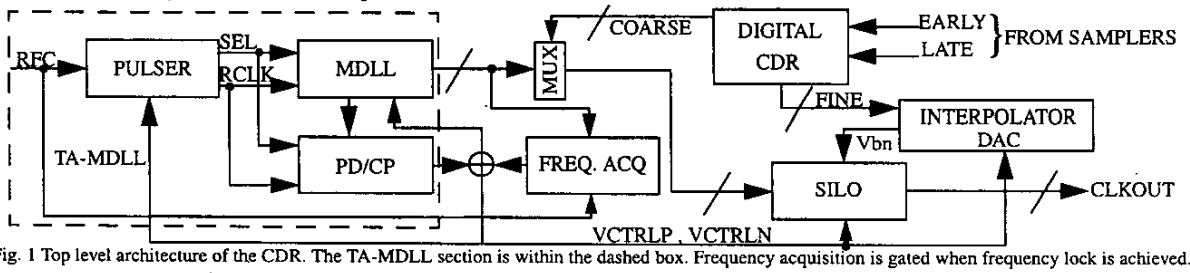

Fig. 1 Top level architecture of the CDR. The TA-MDLL section is within the dashed box. Frequency acquisition is gated when frequency lock is achieved.

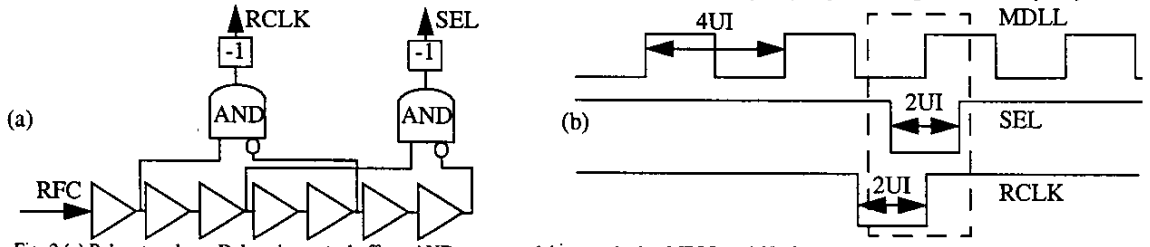

Fig. 2 (a) Pulser topology. Delay elements, buffers, AND gates are delay matched to MDLL and SILO delay elements. (b) Timing diagram showing when SEL pulses low, the clean RCLK is multiplexed in to replace the recirculating edge of the MDLL. Matched delay elements in the Pulser, MDLL, and SILO ensure that the SEL aperture tracks the RCLK and MDLL edge.

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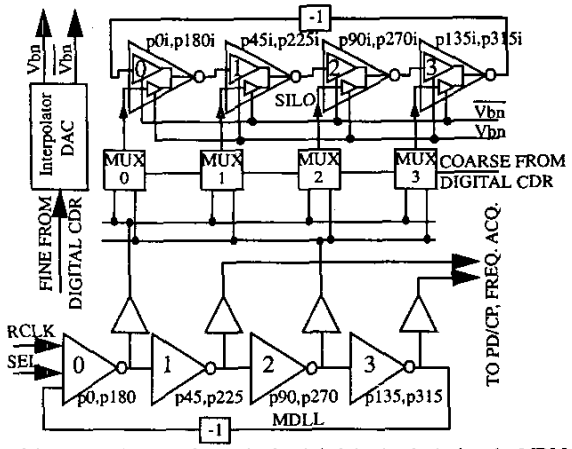

Fig. 3 Top level diagram of how the SILO is injection locked to the MDLL (Pulser not shown).

tracking aperture will also track the edge of the Mth MDLL cycle across PVT and operating frequency. The 250ps (2UI) duration of the SEL aperture is wide enough to counter any MDLL timing uncertainty. To minimize phase error, a combined Phase Detector/Charge Pump circuit (PD/CP) is used [1]. In order to reduce jitter peaking [4] and ripple induced jitter, charge pump current is significantly reduced while being mindful of leakage currents. The output of the PD/CP is VCTRLP that is also sent to a replica bias circuit that provides VCTRLN for biasing NMOS devices. When RCLK is multiplexed in every M clock cycle(s), duty cycle distortion will occur if the MDLL clock edge is offset from its ideal location [5]. In order to prevent the duty cycle distortion induced phase error from propagating through, it is filtered by the SILO via pass gate MUXes as shown in Fig. 3. The amount of filtering is dependent upon the injection strength. Strong injection strength will ensure a wide lock range [6], but without mitigating the phase error and vice-versa. A very weak injection strength is ideal for filtering out the phase error, but is practical only if the MDLL and SILO are well matched to ensure phase lock.

Another advantage of performing injection locking is that by varying the strength of the injected clocks into the SILO delay elements, phase interpolation can be performed (Fig. 3). The 4 pass gate MUXes accept p0, p90, p180, p270 from the MDLL and are controlled by the Digital CDR COARSE bits. If the output of the SILO 1st stage is to be between 0 and 45 degrees, then the outputs of MUX0=p0, MUX1=p0, MUX2=p90, and MUX3=p90. These phases are then injected into the corresponding SILO delay elements. Controlling the efficacy of the injected clocks in advancing or retarding the SILO output phases is performed by trading off Vbn and $\overline{\text{Vbn}}$ against each other. In doing so, the output of the SILO 1st/2nd/3rd/0th stage can be varied between 0/45/90/135 degrees and 45/90/135/180 degrees (single-ended) respectively. This is one advantage of a injection locked quarter-rate architecture over an injection locked half rate architecture, where interpolation can be performed between 45 degree phases as

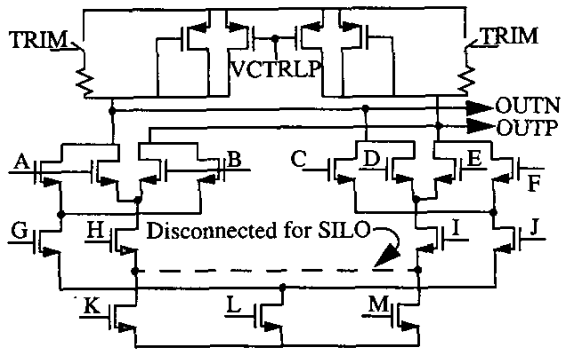

Fig. 4 Generic delay element that can be configured differently for different purposes in several blocks in the CDR. This ensures good matching performance.

opposed to an orthogonal 90 degrees. Note that the Vbn/$\overline{\text{Vbn}}$ connections alternate between the delay elements. The Vbn/$\overline{\text{Vbn}}$ control voltages are sourced from a thermometer coded Interpolator DAC that in turn, obtains its FINE inputs from the Digital CDR. The Digital CDR controls the COARSE and FINE bits after processing the EARLY and LATE signals from the high speed data samplers.

Circuits

The choice of delay element was dictated by the need to use it in the Pulser, MDLL and SILO. A differential pair based element was chosen since it did not require cross-coupled inverters (as in CMOS inverter based oscillators) at its outputs to ensure a true inverse and more importantly, is less susceptible to common mode noise on the supply rail. A differential pair could also be partitioned out as shown in Fig. 4 and Table 1 to easily incorporate a mux. The delay element loads are linear resistors in parallel with linearized symmetric loads [7]. When the symmetric loads are strongly or weakly biased, the VCO gain is high. The linear resistors, when enabled by TRIMF, reduce the VCO gain variation across the

TABLE 1: DELAY ELEMENT CONFIGURATIONS

Inputs	Pulser Buffer	MDLL	SILO
A	IN		
B	IN		
C	LOW	RCLK	LOW
D			INTERP
E		RCLK	INTERP
F			LOW
G		SEL	HIGH
H			
I		SEL	
J			LOW
K	VCTRLN		Vbn
L			VCTRLN
M	LOW		Vbn

VCTRLP voltage range and allow higher frequency operation. Furthermore, linearizing the symmetric loads with the linear resistors also leads to better jitter performance and allow for good matching characteristics across the design. When

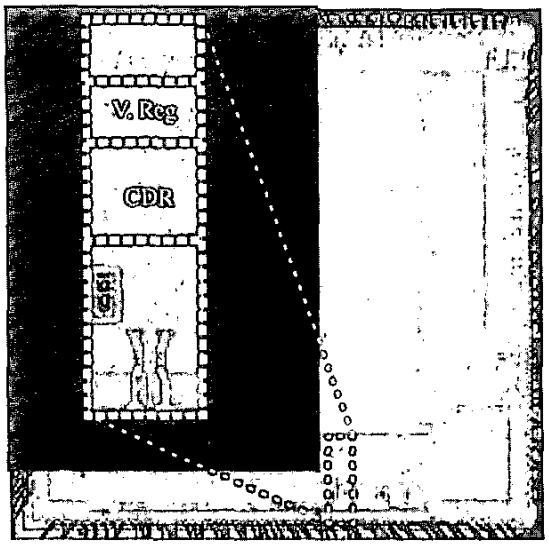

Fig. 5 Die microphotograph of Quad 8Gb/s serializer-deserializer chip. Inset is the zoomed view of a single Receiver, detailing location of CDR.

configured for use in the MDLL, the delay element multiplexes in a clean RCLK edge when SEL is pulsed LOW. This mux is in all stages of the MDLL even though only one of them is really used as a mux. In the Pulser, the delay element is configured as shown in Table 1.

In order to perform fine phase interpolation in the SILO, the tail current source previously biased by VCTRLN in the MDLL is now split into three separate devices biased by VCTRLN, Vbn and $\overline{\text{Vbn}}$. The INTERP inputs receive the injected clocks, whose strengths are controlled by Vbn/$\overline{\text{Vbn}}$. The Vbn/$\overline{\text{Vbn}}$ control voltages perform current steering and can progress from favoring the main SILO oscillator loop to allowing maximum injection strength per delay element. There are 128 phase steps per clock period and the ideal phase step size is 3.9ps at 8Gb/s. Devices are sized to maximize yield when more than 100 transceivers are integrated.

Measured Results

This CDR was used in a 1.2V Quad 8Gb/s serializer/ deserializer chip fabricated in a standard digital 0.13µm CMOS process. The die microphotograph is shown in Fig. 5 where a zoomed up version of a single receiver is shown inset. The CDR and the Voltage Regulator used to suppress power supply noise is shown as partitioned where the Voltage Regulator area incorporates all the MOSFET bypass capacitors used. The total CDR and Voltage Regulator die area is 0.08mm^2 while the total power consumption at 8Gb/s is 33mW with unified 1.2V VDD and GND supply rails.

Fig. 6 shows the performance of 20 unique CDRs as they were statically stepped through all 128 phase steps. The top data points show the peak-to-peak jitter after 3000 hits on the oscilloscope while the lower data points show the phase step size. The interpolator phase steps show compression as they approach a COARSE selection change. The cases of non-monotonicity are undesirable, but as the CDR is a feedback loop, it is acceptable as long as the next phase step is not very large. Nevertheless, these phase step discontinuities must be absorbed in any jitter budget.

Fig. 7(a) shows the jitter histogram of the internal recovered clock (via a single-ended on chip probe) when recovering the

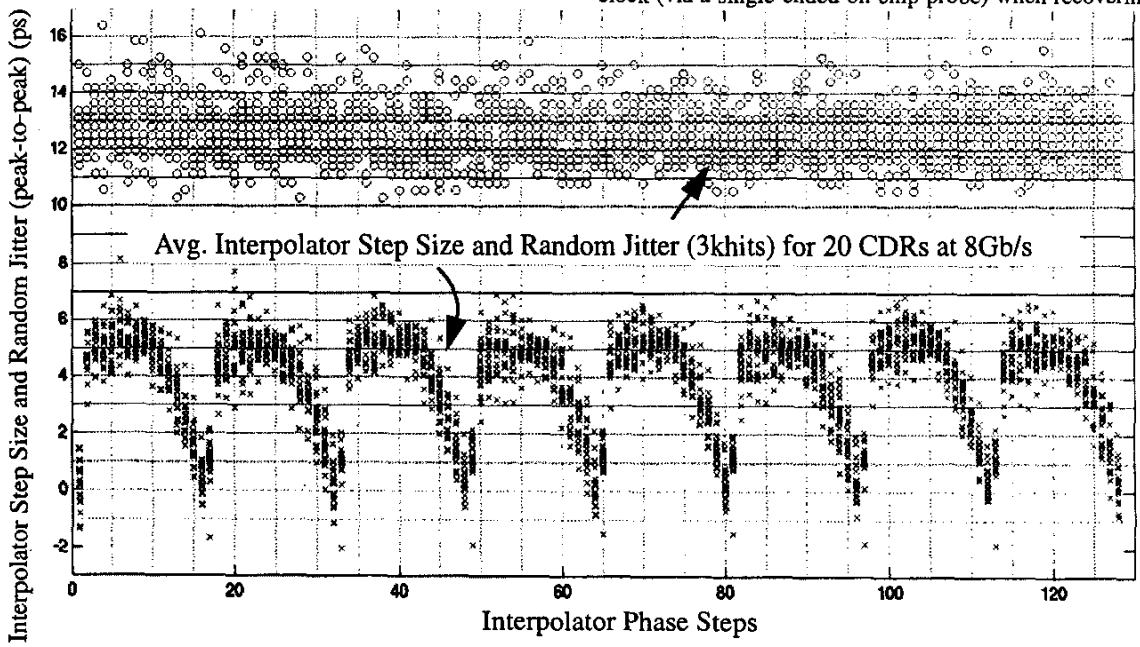

Fig. 6 Transmitter phase step size and random jitter when the CDR is made to statically step through each of the 128 phase steps.

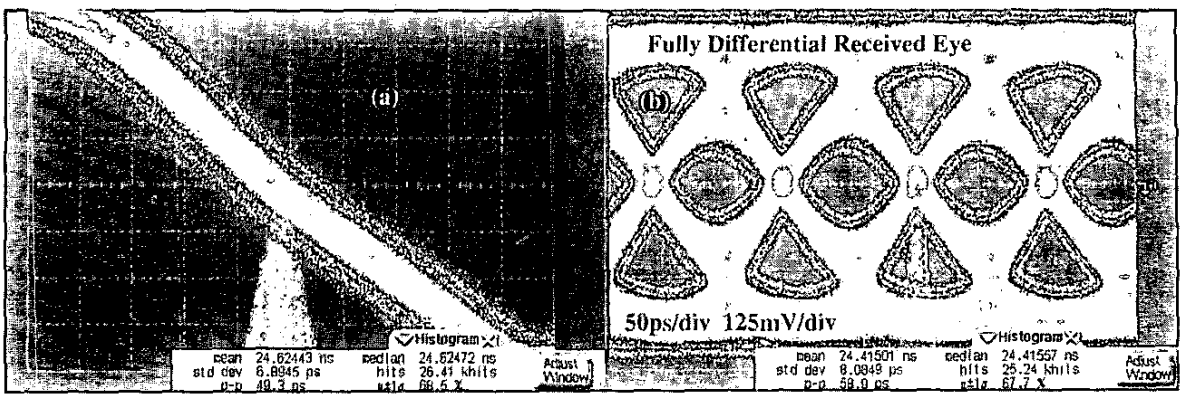

Fig. 7 (a) Jitter histogram of a probed single ended recovered clock, (b) quality of eyes from which the recovered clock is derived.

input data of Fig. 7(b). The input data had a 200ppm bitrate offset to demonstrate *plesiochronous* operation. Recovered clock jitter is 6.9ps rms and 49.3ps peak-to-peak. When the CDR is stopped at a fixed phase step, the Transmitter jitter when sending a ..11001100.. pattern is a good proxy for the quality of the MDLL as a clock multiplier. This is shown in Fig. 8(a) where the 1σ clock jitter is 1.9ps. The 200MHz reference clock used has a 1σ jitter specification of 1ps and phase noise of -120dBc/Hz at a 100kHz offset. Fig. 8(b) shows the 100kHz offset spectrum of the same Transmitter output. At a 100kHz offset, the power is -118db/Hz when the carrier power is -10dB/Hz for a phase noise of -108dBc/Hz. The spurs at 200Mhz and 400MHz offsets are -32dBc/Hz and -43dBc/Hz respectively.

Conclusions

A compact, non-LC, low-power, low-jitter CDR for highly integrated high speed I/Os has been described where a TA-MDLL was used for clock multiplication. Contributions of this work include a Pulser to accurately multiplex in a clean clock edge into the MDLL. The Pulser has been designed to have the maximum sized aperture while tracking the desired MDLL clock edge across PVT and frequency. A multi-faceted delay element design was introduced to successfully perform the task of filtering phase errors from TA-MDLL duty-cycle distortion by injection locking to a SILO. The injection strength is determined by the ratio of the injection bias current to the main delay element bias current. Furthermore, steering the injection currents within the SILO delay elements help perform phase interpolation, obviating the need for downstream interpolation circuitry. A quarter rate architecture lowers digital logic speed for higher yield in large systems and allows easier phase interpolation.

References

[1] R. Farjad-Rad, et-al., "A Low-Power Multiplying DLL for Low-Jitter Multigigahertz Clock Generation in Highly Integrated Digital Chips," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1804-1812, Dec. 2002.

[2] M.-J. E. Lee, et-al., "A Second-Order Semi-Digital Clock Recovery Circuit Based on Injection Locking," *Dig. of Tech. Papers, IEEE ISSCC*, pp. 74-75, Feb. 2003.

[3] R. Farjad-Rad, et-al., "0.622-8Gbps 150mW Serial IO Macrocell with Fully Flexible Preemphasis and Equalization," in press *Dig. of Tech. Papers, IEEE Symposium on VLSI Circuits*, Jun. 2003

[4] M.-J. E. Lee, et-al., "Jitter Transfer Characteristics of Delay-Locked Loops - Theories and Design Techniques," *IEEE J. Solid-State Circuits*, vol. 38, pp. 614-621, Apr. 2003.

[5] G. Chien and P.R. Gray, "A 900-MHz Local Oscillator Using a DLL-Based Frequency Multiplier Technique for PCS Applications," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1996-1999, Dec. 2000.

[6] P. Kinget, et-al, "An Injection-Locking Scheme for Precision Quadrature Generation.," *IEEE J. Solid-State Circuits*, vol. 37, pp. 845-851, Jul. 2002.

[7] J.G. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1723-1732, Nov. 1996

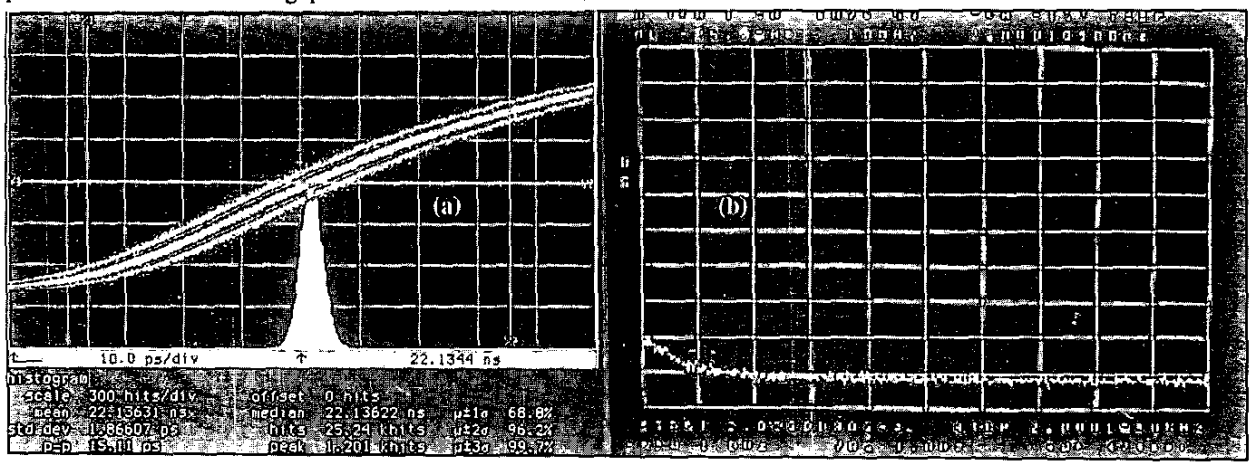

Fig. 8 (a) Jitter histogram of Clock Multiplier as seen through Transmitter output when CDR is stopped (b) phase noise of same waveform