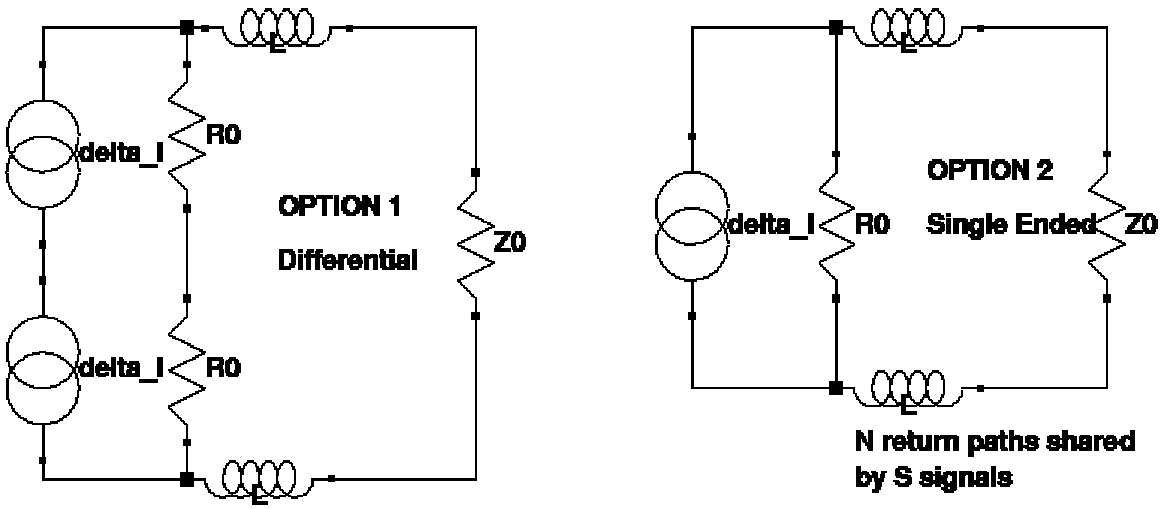
Homework4 Solution

Problem 7-2: **Differential versus Single-Ended Signaling**

The point of the problem is to see how serious the return cross talk due to the lead inductance is and thus to highlight the advantage of differential signaling, which is immune to such cross talk. The given system parameters are repeated below:

Line impedance	Z_0	50	Ω
Source Resistance	R_0	50	Ω
Lead inductance	L	5	NH
Pin count	N	32	Pins
Required data rate	TBR	8	Gb/s



Since the parameters for the first options are already given, (16 differential channels operating at 500 Mb/s,) let's first find the corresponding parameters for the second option. The first step is to list all the constraints and known parameters. The number of single-ended signal pins and return pins are unknown. Assuming that we want the sum of all the pins to be equal to 32, we get equation (7-2-1), where S is the number of signal pins and N is the number of return pins. Also, from the fact that the combined data rate should be 8 Gb/s and the fact that the rise time is half the bit-cell width, we get equation (7-2-2), where B is the bit rate per channel. And from the constraint that k_{xr} be smaller than 0.1, we get equation (7-2-3), which is derived from Equation (7-8) of the textbook, except that Z_{RT} is changed to (Z_{RT}/N) since there are N ground pins. Assuming a constant slope current ramp, Z_{RT} due to the lead inductance is approximately L / t_r.

$$S + N = 32 \quad \Rightarrow \quad N = 32 - S \qquad (7-2-1)$$

$$8E9 = S \times B = S \times \frac{1}{2\,t_r} \quad \Rightarrow \quad \frac{1}{t_r} = \frac{16E9}{S} \qquad (7-2-2)$$

$$k_{XR} \le \frac{(S-1)\,Z_{RT}/N}{(S-1)\,Z_{RT}/N + R_0 + Z_0} = \frac{(S-1)\,Z_{RT}}{(S-1)\,Z_{RT} + N(R_0 + Z_0)} \le 0.1 \qquad (7-2-3)$$

Solving equation (7-2-3) with actual numbers given:

$$\frac{(S-1)\,L/t_t}{(S-1)\,L/t_t + (32-S)(R_0+Z_0)} = \frac{(S-1)\,16E9\,L/S}{(S-1)\,16E9\,L/S + (32-S)(50+50)}$$

$$\Rightarrow \frac{(S-1)\,80}{(S-1)80 + S(32-S)100} \le 0.1 \quad \Rightarrow \quad S \le 25.09$$

$$\textit{Therefore,} \quad \begin{cases} S \le 25 \\ N \ge 7 \end{cases} \quad \Rightarrow \quad \begin{cases} B = 320\,Mbps/channel \\ t_r = 1.5625\,ns \end{cases}$$

So, the number of signal lines has increased by 9, and the required bandwidth/pin has decreased by about 1/3.

Now, let's compare the noise margins of these two options. Since neither the voltage swing nor the current swing is given, let's solve the margins in terms of ΔI, the current swing on the transmission line (not the swing at the current source). Notice that ΔI is defined as the signal swing of each wire. Thus, the gross margin for option 1 is twice that for the option 2, since the effective signal swing is twice ΔI, the signal swing of a single line, which is the same for the two options. .

$$Gross\_MARGIN_1 = \Delta I\, Z_0 \qquad Gross\_MARGIN_1 = \frac{\Delta I\, Z_0}{2}$$

Finding the net margin for option 1: (Notice that due to our assumptions, twice ΔI is used for proportional noise while V_{NI} is the same as for the single ended case. This is not a very realistic assumption, and normally, each component of V_{NI} and K_N needs to be evaluated to yield new V_{NI} and K_N. More explanation at the end of this problem.)

$$V_{N1} = V_{NI} + K_N(2\Delta I\, Z_0)$$

$$\begin{aligned} \rightarrow \quad Net\_MARGIN_2 &= Gross\_MARGIN_1 - V_{N1} \\ &= \Delta I\, Z_0 - V_{NI} + K_N(2\Delta I\, Z_0) \\ &= \Delta I\, Z_0(1-2K_N) - V_{NI} \\ &= 35\Delta I - 20mV \end{aligned}$$

Now, calculating the net margin for option 2, we include the return cross talk factor. K_{XR} is approximately 0.1 since we chose S very close to the break-even point of (7-2-3).

$$V_{N2} = V_{NI} + K_N(\Delta I\, Z_0)$$

$$\begin{aligned} \rightarrow \quad Net\_MARGIN_2 &= Gross\_MARGIN_2 - V_{N2} - V_{XR} \\ &= \frac{\Delta I\, Z_0}{2} - V_{NI} + K_N(\Delta I\, Z_0) - 0.1 Z_0\, \Delta I \\ &= \Delta I\, Z_0(0.5 - K_N) - V_{NI} - 5\Delta I \\ &= 12.5\Delta I - 20mV \end{aligned}$$

Note that if we ignore the V_{NI} term, the (Net_margin / ΔI) term for the first option is more than twice of that for the second option.

The table below summarizes the parameters for the two options:

	1st Option	2nd Option
	Differentially Driven	Single Ended with multiple returns
t_r	1nsec	1.5625nsec
# of channels	16	25
rate/channel	500Mbps	320Mbps
Net_Margin	35 ΔI – 20mV	12.5 ΔI – 20mV

The pros and cons for the two options are shown in the following table. Basically, the differential signaling method has all the advantages listed on page 329 of the textbook. Determining which channel is better really depends on the application at hand. Differential signaling seems to have superior noise margin as well as many advantages over single-ended signaling. However, it may be difficult to achieve 500Mbps/pin performance even with improved noise margin. It may be desirable to have a slower rise time for the constraint outside the chip.

1st Option	2nd Option
• no return crosstalk -> independent channels • Larger noise margin for the same ΔI • Faster rise time for same effective swing • Half the power for same effective swing	• less sensitive to clock jittering • Smaller reflection from discontinuities on the line

We have used the same V_{NI} and twice the K_N for the differential signaling. However, in the real-world applications, it's important to analyze each component of the noise sources to see how they're different in differential signaling case. The actual analysis depends on number of assumptions and environment, and an example is shown below. Assume the noise characteristics of Table 7-4 and 7-5 of page 310.

V_{rs}, receiver sensitivity, as well as V_{ro}, receiver offset, are not cancelled by driving the line differentially, and this part of V_{NI} will remain the same.

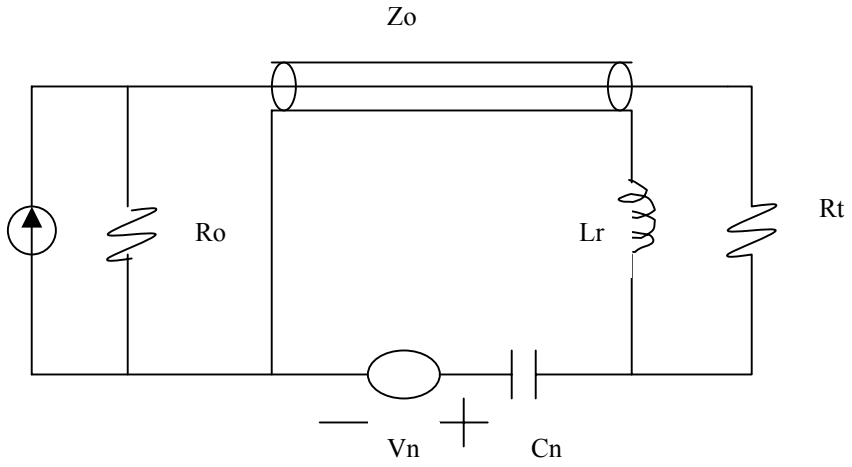
Most of V_{eo}, external power supply noise, will be rejected, as it affects both lines equally. Only a small fraction of this noise, the part that is not rejected, will add to V_{NI}.
ls
K_{xt}, cross talk from other signals, will be halved, assuming it affects only one line of the differential pair (the line closer to the aggressor) and not the other line.

K_r, reflection from previous cycle, is unchanged. It affects each line of the differential pair equally.

K_{to}, transmitter offset, is unchanged. It affects both lines equally, but still reduces the signal swing available.

Problem 7.4 Power Supply Noise:

A signaling system with capacitively coupled power supply noise is illustrated in Figure below. Give an expression for the amount of supply noise, Vn , that appears about the termination resistor, Rt, as a function of frequency and component values. Suppose Zo=Rt=50 ohm and Ro=1Kiloohm,Cn = 5pF, Lr = 5 nH, and Vn = 500 mV. How much signal swing is required to keep the power-supply noise les than 10% of the signal swing across the spectrum from Dc to 1 GHz?



Solution:

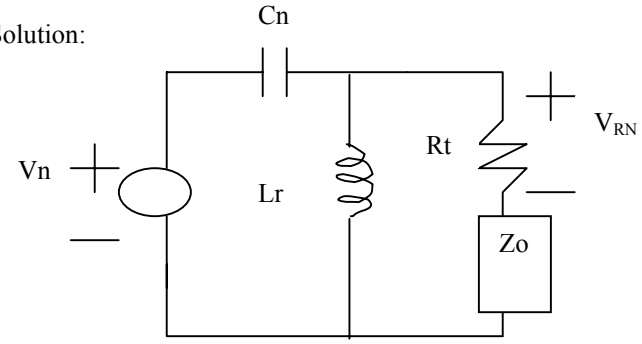


Fig : Equivalent circuit for Power Supply Noise:

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$$V_{RN} = \frac{V_N \ (Zo \ j\omega L_R)}{2 Z_o \ j\omega L_R + (2 Z_o + j\omega L_R)(j\omega C)^{-1}}$$

$$= \frac{V_N \ 4\pi^2 Z_o L_R C f^2}{8\pi^2 Z_o L_R C f^2 + 2 Z_o + j \ 2\pi f L_R}$$

$$= \frac{-2.5 \times 10^{-18} f^2 \ \text{Volts}}{-98.5 \times 10^{-18} f^2 + 100 + j \ 31.4 \times 10^{-9} f}$$

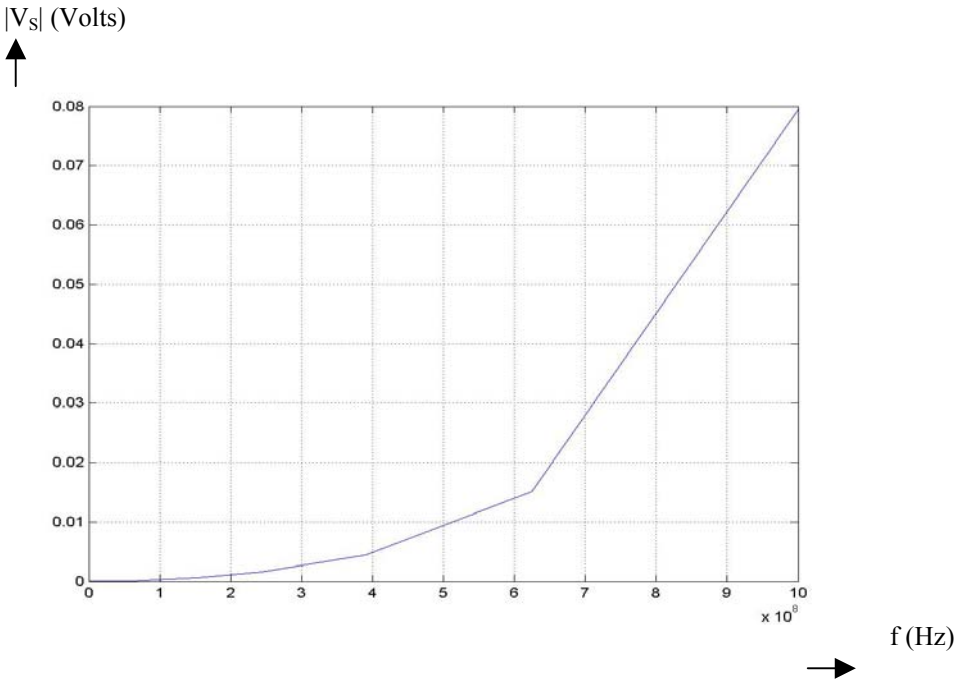
To get a rough idea of how much swing required varies with frequency :

Let the voltage swing that we get at the receiver be Vs .

We want $0.1\ V_S > V_{RN}$

⇨ $V_S > 10V_{RN}$

Plotting the value of V_S for f=0 to f= 1GHz



You can also do this by calculating how much swing we will get at the output (taking into account the reflections at either end).

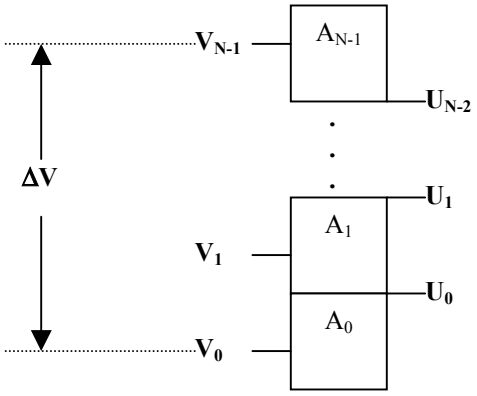
Problem 7-8: **Multilevel Signaling**

This problem is modified as follows:

a) What's the maximum number of signal levels supportable and what's the corresponding signal swing?

<Assumption> The Table 7-4 and 7-5 gives V_{NI} = 18mV and K_N = 0.25. I assume that these two quantities are true even for the multilevel signaling.

a) The symbols for multilevel signaling is shown in Figure 7-39 of the textbook and repeated here for convenience.



Let $dV = U_j - V_j$
➔ $\Delta V = (N-1)(2dV)$

The noise requirement is
$dV < V_N$
where V_N is worst case noise

From here, it's evident that we don't want the noise to be bigger than dV, in which case a signal can be misinterpreted. The way to find the maximum number of signal levels is very straightforward and proceeds as shown below.

$$V_N = V_{NI} + K_N \Delta V = 23mV + (0.25)\Delta V$$

$$dV = \frac{\Delta V}{2(N-1)} > V_{NI} + K_N \Delta V$$

$$\rightarrow \qquad \Delta V > \frac{2V_{NI}(N-1)}{1-2(N-1)K_N} \qquad (7-8-1)$$

This last expression is very similar to familiar inequality such as Eqn (7-3) of the textbook, and for the case of binary signaling, it degenerates to Eqn (7-3) as expected. Now, looking at this inequality, the constraint on N is obvious. As N is being increased, the denominator of the right hand side will eventually become negative. Since it doesn't make sense to have negative denominator in this context, this will give us the maximum number of N possible with given K_N. That is

$$1-2(N-1)K_N > 0 \quad \rightarrow \qquad N < \frac{1}{2K_N} + 1 = 3 \qquad (7-8-2)$$

For three level signaling, N=3, equation (7-8-2) gives required signal swing of infinity, which obviously is not possible. Therefore, the maximum signal level is **N=2**. Applying equation (7-8-1), we get the required signal swing of **$\Delta V > 72mV$**.

Note: Using (7-8-2), we can see that V_{NI} doesn't come into play when determining the maximum number of signal levels. It intuitively makes sense since independent noise can be overcome by employing higher ΔV. However signal dependent noise scales with ΔV, whereas the absolute noise margin is only $dV = \Delta V/(2(N-1))$. One can visualize it using the figure on the previous page how there must be certain limit where simply increasing ΔV can't help at all. As a result, even though the multilevel signaling multiplies both V_{NI} and K_N as shown in eqn (7-8-1), only K_P determines the maximum level of signals and thus one can say that multilevel signaling accentuates the effect of proportional noise.