Homework 3 - Solutions

1 Problem 6-4 (Dally and Poulton)

Capacitive Cross Talk to Dynamic Circuits:

Consider the 3-mm-long on-chip bus from Exercise 6-3. In this case, however, you are precharging the bus and selectively discharging each bit with the circuit shown Figure 6-30(a). (a) What happens to the voltage on bit 2 if, after precharging, adjacent bits 1 and 3 are pulled low whereas bit 2 is allowed to float (draw a dimensional sketch). Assume that the selected pulldown chain can be modeled by a 1-kΩ resistor and ignore the capacitance of the pulldown chains. What happens if bit 2 is pulled up with a "keeper," as shown in Figuer 6-30(b), which you can model as a 2-kΩ resistor? Draw a second sketch.

(a) For this problem we have a 3-mm-long on-chip bus. We derive our capacitance values from Table 6-2: The coupling capacitance between each of the bitlines is:

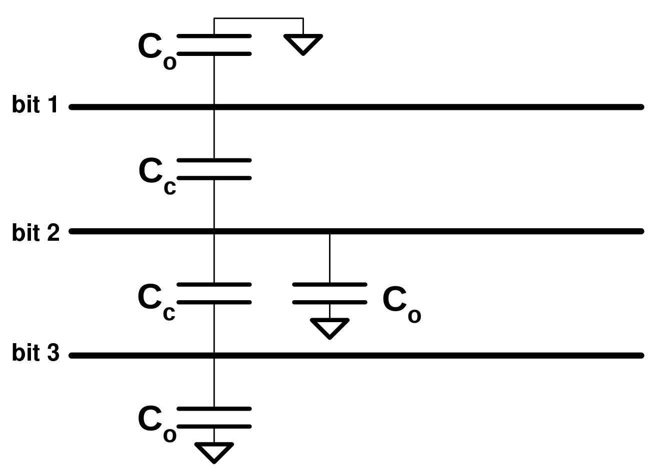
$$C_c = 0.03\frac{fF}{\mu m} \times 3mm = 90fF$$

The capacitance to other wires, the wires above and below the bit lines is:

$$C_o = 2 \times (0.03\frac{fF}{\mu m} + (2 \times 0.01\frac{fF}{\mu m})) \times 3mm = 300fF$$

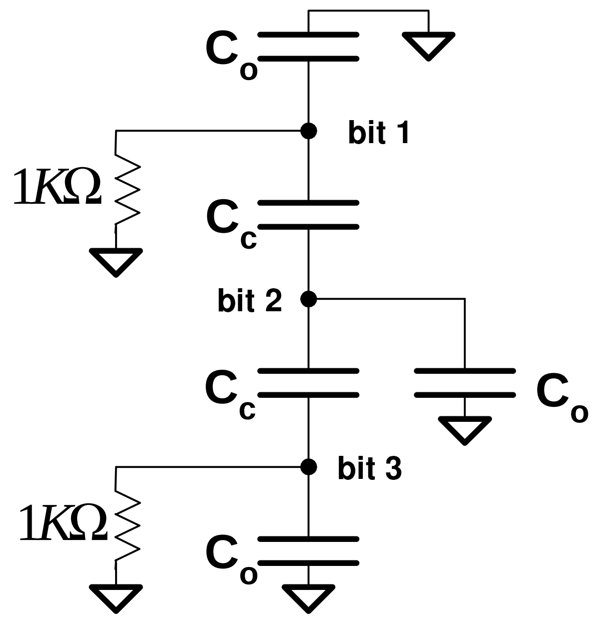
The fringing field ($0.01\frac{fF}{\mu m}$) is multiplied by 2 for fringing from each side of the bit line. The entire parallel plate capacitance, the capacitance inside the parantheses, is multiplied by 2 to account for the wires above **and** below the current plane.

So, we model our bitlines as follows:

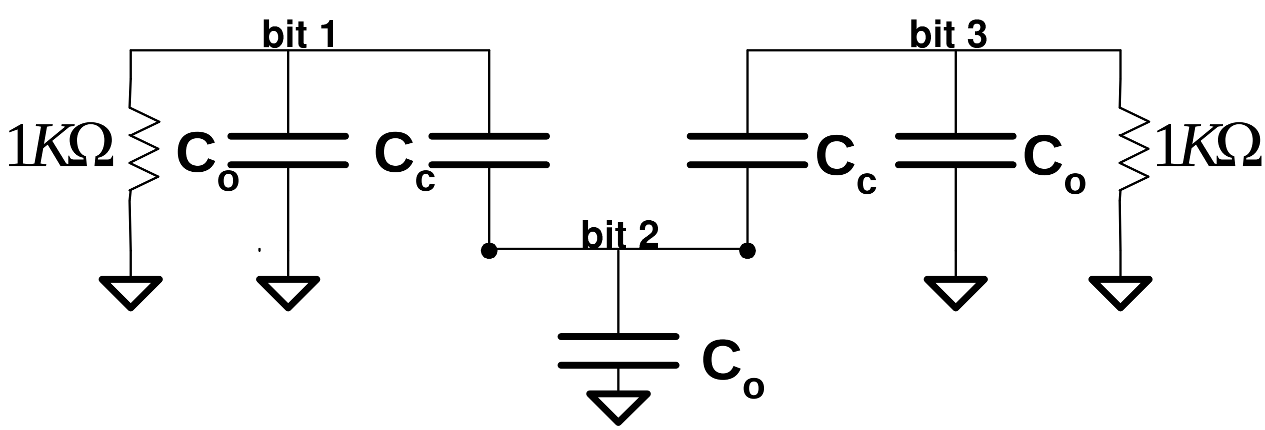


Note: We are ignoring the coupling capacitance to other neighboring and non-adjacent bit-lines.

Initially all of the bitlines are precharged to a value of 1 V. We then pull bits 1 and 3 down with the pull-down circuit shown, which we model as a 1 kΩ resistor. Constructing an equivalent circuit, we have:



Rearranging for clarity, we have:



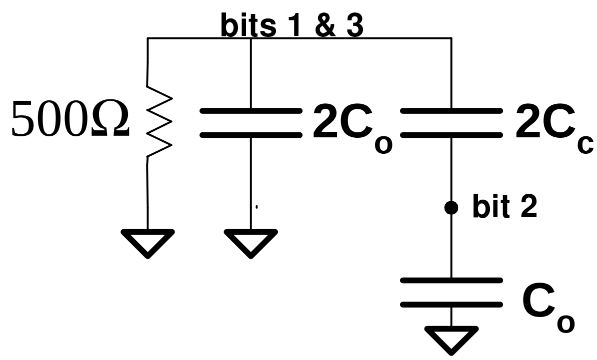
Since the voltages on lines 1 & 3 will be exactly the same, we draw an equivalent circuit as:

We now solve for the equivalent resistance that the 500-Ω pull-down chain sees:

$$C_{eq} = 2C_o + \frac{2C_cC_o}{2C_c + C_o} = 600fF + 112.5fF = 712.5fF$$

Thus, the RC time constant of our circuit is:

$$\tau = 500\Omega * 712.5fF = 356ps$$



Solving for the voltage for bits 1 and 3 we get:

$$\boxed{V_{bits1\&3}(t) = e^{-\frac{t}{\tau}} = e^{-\frac{t}{356ps}}}$$

The capacitors act as voltage dividers between the bits1&3 lines and the bit 2 line. So, the voltage lost by the bit 2 line is:

$$\boxed{\frac{2C_c}{2C_c + C_o} \times \Delta V_{bits1\&3} = 0.375 \times -1V = -0.375V}$$

Thus, the final voltage on the bit 2 line will be 1V - 0.375 V = 0.625V. The resulting equation for the voltage on bit line 2 is:

$$\boxed{V_{bit2}(t) = 0.625 + 0.375e^{-\frac{t}{356ps}}}$$

Below are the waveforms of the voltages seen on bit-lines 1&3 and on bit-line 2 as described by the equations above.

Note: we achieve this exact same solution using KCL anc KVL and solving the differential equations in the s-domain.

(b) Now we add a 2-kΩ pull-up "keeper" on bit-line 2. With this configuration, we have the pull-down circuit pulling down the voltage on bit-line 2 and the "keeper" circuit pulling up the voltage on bit-line 2. We can approach this problem in two ways: (1) Assume the time constant of the pull-up circuit is larger than the time constant of the pull-down circuit, or (2) Solve for the exact solution in the s-domain. In the first option we de-couple the effects of the pull-up and pull-down circuit. The following is the solution using the assumptions of option 1.

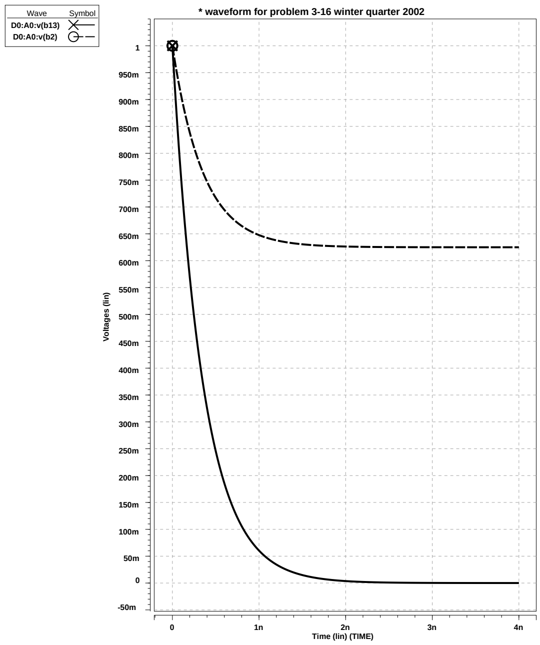
If we assume the time constant of the pull-down network, 356ps, is significantly smaller than the time constant of the pull-up "keeper", we can say that bit-lines 1&3 reach their final value, 0 V, well before the pull-up network takes effect.

Thus, the effective capacitance seen by the 2-kΩ pull-up circuit will be $2C_c$ in parallel with C_o:

$$\boxed{C_{eff} = 2C_c + C_o = 180fF + 300fF = 480fF}$$

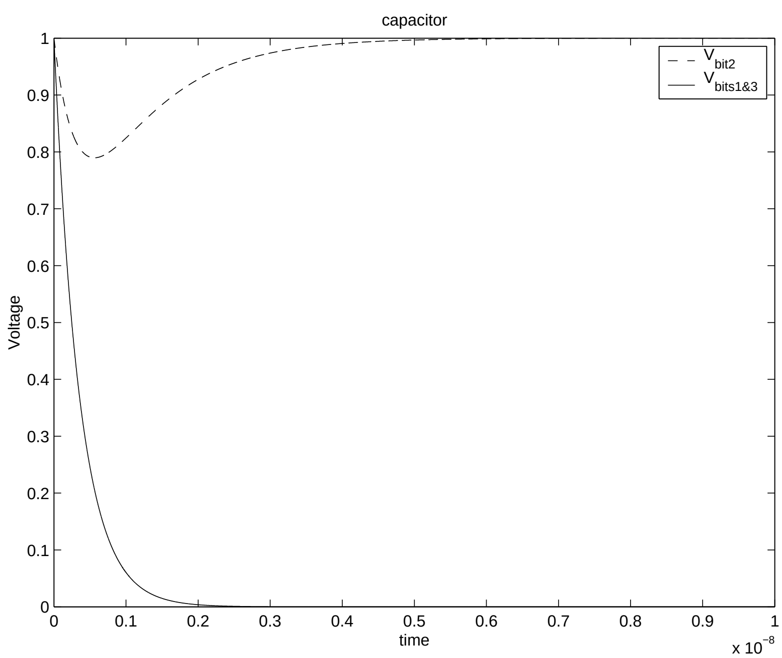
So, our time constant for the pull-up network, using the assumptions stated above, will be:

$$\boxed{\tau = RC_{eff} = 2k\Omega \times 480fF = 960ps}$$

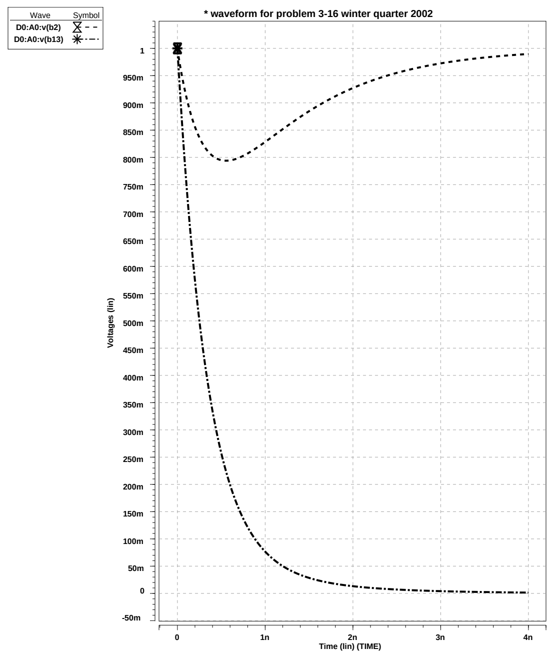


Choosing our constants to obtain the correct response, the voltage seen on bit-line 2 will be:

$$\boxed{V_{bit2}(t) = 1 - (0.6e^{-\frac{t}{960ps}} - 0.6e^{-\frac{t}{356ps}})}$$



Below is the actual response of the circuit.



A comparison between the actual voltage waveform on bit-line 2 and our estimated waveform on bit-line 2 shows that the estimation used in the first option gave us a close approximation to the actual behavior.

2 Problem 6-6 (Dally and Poulton)

Transmission-Line Cross Talk Using Propagation Modes:

Another way to analyze cross talk is to consider the differential and common-mode impedances of a coupled pair of lines. Putting a unit step into line 1 while holding line 2 at a steady value, $V_1 = U(t)$, $V_2 = 0$, is the equivalent of sending a differential voltage of $V_D = -0.5\ \Delta V = -0.5\ U(t)$, and a common-mode voltage of $V_C = 0.5U(t)$ into the quiet line, line 2. The cross talk can then be calculated as the superposition of the even and odd mode responses of the quiet line.

Using Eqs. (3-59) and (3-60), calculate the differential and common-mode impedances of the coupled line assuming the geometry from the second line of Table 6-3. Compute the differential and common-mode response of the quiet line to a step on the driven line assuming a source impedance and a termination impedance of Z_o. From these responses compute the near-end and far-end coupling coefficients.

We are given the first 2 entries in the following table and we obtain the following 5 entries from table 6-3 in the book. We will derive the rest of the values in the table.

Coupled length	1 m
t_r	500 ps
C	137 $\frac{pF}{m}$
C_m	3 $\frac{pF}{m}$
L	240 $\frac{nH}{m}$
M	18.5 $\frac{nH}{m}$
Z_o	42 Ω
$k_c x$	0.021
$k_l x$	0.077
$k_f x$	-0.028
$k_r x$	0.025
Velocity_{even}	1.70 $\times 10^{-8} \frac{m}{s}$
Velocity_{odd}	1.80 $\times 10^{-8} \frac{m}{s}$
$\text{Velocity}_{overall}$	1.74 $\times 10^{-8} \frac{m}{s}$
$T_{line(even)}$	5.89 ns
$T_{line(odd)}$	5.57 ns
$T_{line(overall)}$	5.73 ns

We begin by calculating the even and odd mode impedances:

$$Z_{EVEN} = \sqrt{\frac{L+M}{C-C_m}} = \sqrt{\frac{240\frac{nH}{m} + 18.5\frac{nH}{m}}{137\frac{pF}{m} - 3\frac{pF}{m}}} = \boxed{43.9\Omega}$$

$$Z_{ODD} = \sqrt{\frac{L-M}{C+C_m}} = \sqrt{\frac{240\frac{nH}{m} - 18.5\frac{nH}{m}}{137\frac{pF}{m} + 3\frac{pF}{m}}} = \boxed{39.8\Omega}$$

We now calculate the even and odd mode signals of A, the aggressor line, and Q, the quiet line as shown below.

$$V_{A(even)} = 1V \times \frac{Z_{even}}{42\Omega + Z_{even}} = 1V \times \frac{43.9\Omega}{42\Omega + 43.9\Omega} = \boxed{0.511V}$$

$$V_{A(odd)} = 1V \times \frac{Z_{odd}}{42\Omega + Z_{odd}} = 1V \times \frac{39.8\Omega}{42\Omega + 39.8\Omega} = \boxed{0.487V}$$

$$V_{Q(even)} = 1V \times \frac{Z_{even}}{42\Omega + Z_{even}} = 1V \times \frac{43.9\Omega}{42\Omega + 43.9\Omega} = \boxed{0.511V}$$

$$V_{Q(odd)} = -1V \times \frac{Z_{odd}}{42\Omega + Z_{odd}} = -1V \times \frac{39.8\Omega}{42\Omega + 39.8\Omega} = \boxed{-0.487V}$$

Now we calculate the total signal seen on lines A and Q.

$$V_{A(total)} = V_{A(even)} + V_{A(odd)} = 0.511V + 0.487V = \boxed{1V}$$

$$V_{Q(total)} = V_{Q(even)} + V_{Q(odd)} = 0.511V - 0.487V = \boxed{0.024V}$$

Thus, our reverse cross-talk, k_{rx}, is:

$$\boxed{k_{rx} = \frac{0.024V}{1V} = 0.024}$$

This compares well with the value given in the book and the value we calculate from the inductance and impedance,

$$k_{cx} = \frac{C_c}{C_s + C_c} = \frac{C_c}{C} = \frac{3pF}{137pF} = 0.0219$$

$$k_{lx} = \frac{M}{L} = \frac{18.5nH}{240nH} = 0.0771$$

Thus, we get:

$$\boxed{k_{rx} = \frac{k_{cx} + k_{lx}}{4} = 0.0247}$$

Similarly, from our calculations, we find that k_{fx} is as given below. We will verify this forward cross-talk coefficient in the following analysis.

$$\boxed{k_{fx} = \frac{k_{cx} - k_{lx}}{2} = -0.0276}$$

We solve for our forward cross-talk coefficient, k_{fx}, and verify the number calculated above. First we solve for the magnitude of the even and odd mode voltages at the far-end of the line using the telegrapher's equation.

$$V_{Qfar-end(odd)} = V_{Qnear-end(odd)} \times (1 + k_{far-end(odd)}) = -0.487V \times (1 + \frac{42\Omega - 39.8\Omega}{42\Omega 39.8\Omega}) = \boxed{-0.5V}$$

$$V_{Qfar-end(even)} = V_{Qnear-end(even)} \times (1 + k_{far-end(even)}) = 0.511V \times (1 + \frac{42\Omega - 43.9\Omega}{42\Omega + 43.9\Omega}) = \boxed{0.5V}$$

We calculate the the velocity of the even and odd mode waves:

$$v_{even} = \sqrt{\frac{1}{L_{even}C_{even}}} = \sqrt{\frac{1}{(L+M)(C-C_m)}} = \boxed{1.70 \times 10^8 \frac{m}{s}}$$

$$v_{odd} = \sqrt{\frac{1}{L_{odd}C_{odd}}} = \sqrt{\frac{1}{(L-M)(C+C_m)}} = \boxed{1.80 \times 10^8 \frac{m}{s}}$$

$$v_{overall} = \sqrt{\frac{1}{LC}} = \sqrt{\frac{1}{240nH \times 137pF}} = \boxed{1.74 \times 10^8 \frac{m}{s}}$$

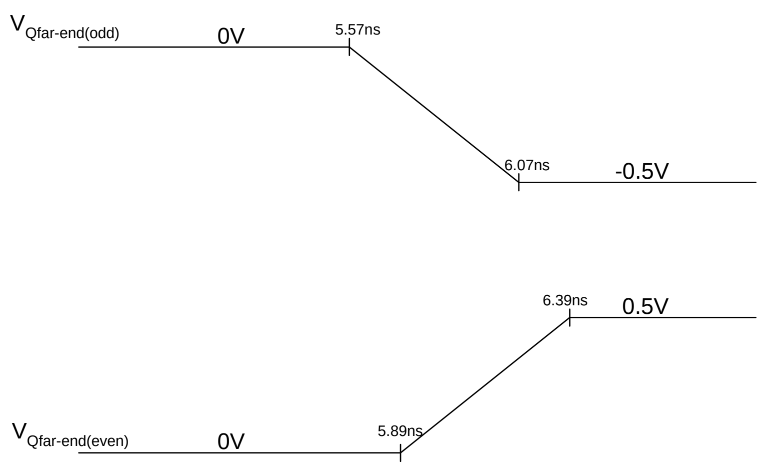
We find the time it takes for the even and the odd mode waves to travel down the line:

$$T_{even} = \frac{Length}{velocity_{even}} = \frac{1m}{1.70 \times 10^8 \frac{m}{s}} = \boxed{5.89ns}$$

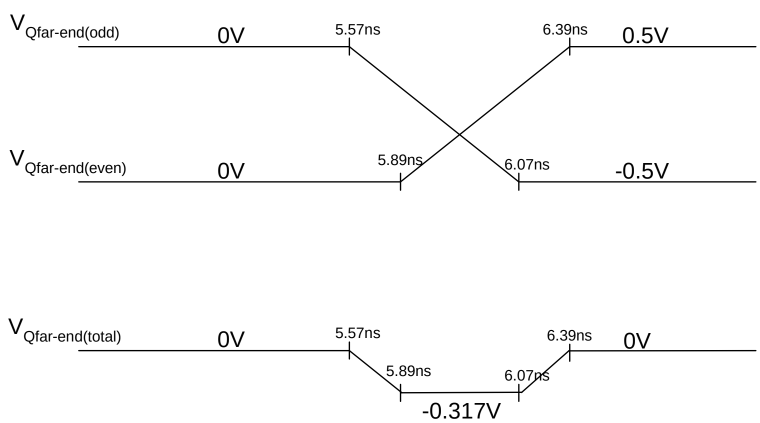
$$T_{odd} = \frac{Length}{velocity_{odd}} = \frac{1m}{1.80 \times 10^8 \frac{m}{s}} = \boxed{5.57ns}$$

$$T_{overall} = \frac{Length}{velocity_{overall}} = \frac{1m}{1.74 \times 10^8 \frac{m}{s}} = \boxed{5.74ns}$$

Thus, we get the following waveforms for the even and odd signals at the far-end of the quiet line:



So our total voltage at the far-end of line Q is as shown on the following page:



With the equation from the Figure 6-12, page 274, repeated here for convenience, we get:

$$V_{Qfar-end_{max}} = \frac{k_{fx} t_x}{t_r}$$

Rearranging, we have:

$$k_{fx} = \frac{V_{Qfar-end_{max}} t_r}{t_x} = \frac{-0.317 \times 500ps}{5.74ns} = \boxed{-0.0276}$$

which is exactly the value we obtained empirically above.

3 Problem 6-13 (Dally and Poulton)

Worst-Case Noise Analysis:

(a) With the given parameters, our signaling system won't work. We have a signal swing, ΔV, of 500 mV. Thus, our gross margin, $V_{GM} = \frac{\Delta V}{2} = 250mV$.

To evaluate our system, we want the highest signal-to-noise ratio, SNR, and equivalently, the highest margin ratio, MR, as defined below:

$$SNR = \frac{V_{swing}}{2 \times V_N}$$

$$MR = \frac{V_{NM}}{V_{GM}}, where V_{NM} = NetMargin = V_{GM} - V_N$$

Using the Margin Ratio and the SNR is a much more robust way of evaluating noise in our system than just looking at the noise margin, V_{NM}.

Accounting for our fixed noise sources in the order they were given in the problem, we compute the total bounded noise as follows:

$$V_N = V_{NI} + K_N \times V_{swing} = 100mV + 100mV + 100mV + 0.2(500mV) + 0.1(500mV) = \boxed{450mV}$$

This value is 200mV greater than V_{GM} and will leave us with a negative net margin, V_{NM}, of -200mV, a signal-to-noise ratio, SNR, of $\frac{500mV}{2 \times 450mV} = \boxed{0.56}$ and a margin ration, MR, of $\frac{-200mV}{250mV} = -0.8$. With the net margin greater than our gross margin and the SNR less than 1, our system **won't pass a worst-case noise analysis**.

(b) Now we must choose 2 of the 5 given options to enable our system to pass a worst-case analysis.

We can run an exhaustive search over each pair of algorithms to find the combination of two options that gives us the highest SNR (and MR).

	Sys	1&2	1&3	2&3	3&4	1&5	2&5	3&5	1&4	2&4	4&5
Signal Swing	0.5	1.0	1.0	0.5	0.5	1.0	0.5	0.5	1.0	0.5	0.5
Rec Offset	0.1	0.01	0.1	0.01	0.1	0.1	0.01	0.1	0.1	0.01	0.1
Rec Sens	0.1	0.01	0.1	0.01	0.1	0.1	0.01	0.1	0.1	0.01	0.1
Transm Offset	0.1	0.1	0.1	0.1	0.1	0.03	0.03	0.03	0.1	0.1	0.03
V_{ni}	0.3	0.12	0.3	0.12	0.3	0.23	0.05	0.23	0.3	0.12	0.23
X-talk Coeff	0.2	0.2	0.05	0.05	0.05	0.2	0.2	0.05	0.2	0.2	0.2
ISI	0.1	0.1	0.1	0.1	0.025	0.1	0.1	0.1	0.025	0.025	0.025
K_n	0.3	0.3	0.15	0.15	0.075	.3	0.3	0.15	0.225	0.225	0.225
Noise V_n	0.45	0.42	0.45	0.195	0.338	0.530	0.2	0.305	0.525	0.233	0.343
SNR	0.56	1.19	1.11	1.28	0.74	0.94	1.25	0.82	0.95	1.07	0.73
MR	-0.8	0.16	0.10	0.22	-0.35	-0.06	0.2	-0.22	-0.05	0.07	-0.37

We choose **options 2&3** since, as shown above, the combination of options 2 and option 3 gives us the highest SNR (and MR).

We could also approach this problem in this manner: We notice that in our original system, the independent noise sources (300mV) dominate the proportional noise sources (150mV). So, reducing the noise due to the independent noise sources is necessary.

Of the two independent noise source reductions, options 2 and 5, we would choose option 2 (V_{ni} = 120mV vs. 270mV of option 5). Now our proportional noise sources (150mV) dominate our independent noise sources (120mV). So, we have a choice of reducing our proportional noise sources or increasing the signal swing.

Of the two proportional noise source reductions, options 3 and 4, we would choose option 3 (K_n = 0.15 vs. 0.225 of option 4).

However, since the voltage swing affects these proportional noise sources and our overall margin, we must take option 1 as a possibility as well. Now we compare our 3 possibilities:

$$options 2\&3 : V_N = 120mV + 0.15(500mV) = 195mV, SNR = 1.28, MR = 0.22$$

$$options 1\&3 : V_N = 120mV + 0.3(1V) = 420mV, SNR = 1.19, MR = 0.16$$

$$options 1\&2 : V_N = 300mV + 0.15(1V) = 450mV, SNR = 1.11, MR = 0.1$$

We choose **options 2 and 3**, as before, which has the largest SNR and MR.

4 Problem 6-14 (Dally and Poulton)

Statistical Noise Analysis: Consider a system with ΔV = 500mV. The signal is corrupted by fixed-noise sources with total V_{NI} = 100mV and K_N = 0.2. In addition, there is additive Gaussian noise with a magnitude of 10mV rms. Calculate the BER for this system.

Our gross margin, V_{GM} is $\frac{\Delta V}{2} = 250mV$. And our total bounded noise is:

$$V_N = V_{NI} + K_N V_S = 100mV + 0.2(500mV) = 200mV$$

Our Voltage Signal to Noise Ratio, VSNR, is:

$$VSNR = \frac{\frac{\Delta V}{2} - V_N}{V_{rms}} = \frac{50mV}{10mV} = 5$$

Thus, our Bit Error Rate, BER is:

$$P(error) = e^{-\frac{VSNR^2}{2}} = \boxed{3.73 \times 10^{-6} = BER}$$